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Activity Results Report:

"Design and Development of battery-free low maintenance Transient IoT Environment Monitoring System"

This project is centered around the development of a battery-free IoT system for environmental monitoring in transient and remote conditions. The goal is to build a robust, self-sustaining device that captures critical environmental data without relying on conventional batteries or frequent human intervention.

The system leverages energy harvesting techniques (such as solar, vibration, or RF harvesting) to power ultra-low-power sensors and communication modules. These sensors are designed to monitor key environmental parameters like temperature, humidity, air quality, or soil moisture depending on the application. The device includes intelligent power management circuitry that activates sensing and data transmission only when sufficient energy is available, enabling long-term deployment even in unpredictable environments.

The architecture consists of modular components with an ultra-low-power microcontroller, onboard storage, and a compact wireless communication module (e.g., BLE, LoRa, or satellite), allowing the collected data to be reliably sent to a cloud server or central gateway. The system is built using durable, lightweight materials and can be deployed quickly in temporary or mobile installations without the need for infrastructure support. Applications include environmental research, smart agriculture, industrial safety, disaster recovery, and temporary field operations where wiring or battery replacement is impractical. This approach ensures reduced maintenance costs, improved flexibility, and scalable data acquisition for real-time environment monitoring across dynamic locations.

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1. Executive Summary

1.1 Project Overview

This project involves the development of an innovative **checkpointing-free intermittent computing system** designed to operate reliably during frequent power failures. The system, based on the Intermittent-OS architecture, comprises three integrated subsystems:

- A **Mixed-Volatility Memory Architecture** leveraging MSP430FR5994's FRAM and SRAM capabilities
- A **Checkpointing-Free Recovery System** that maintains computation progress without traditional state saving
- An **Energy Harvesting Interface** supporting solar, RF, vibration, and thermal energy sources

The primary purpose is to enable continuous computation in environments where power availability is sporadic and unpredictable, eliminating the 20-50% overhead associated with traditional checkpointing approaches.

1.2 High-Level System Architecture

The system architecture consists of:

Hardware Platform:

- MSP430FR5994 microcontroller with 256KB FRAM and 8KB SRAM
- Integrated voltage monitoring via ADC
- Energy harvesting interface with capacitor storage
- Mixed-volatility memory partitioning

Software Components:

- **Intermittent-OS Core**: Modified intermittent execution support
- **Data Manager**: Handles consistency without explicit checkpoints

- **Recovery Handler**: Provides instant restoration after power failures
- **Task Scheduler**: Manages atomic task execution boundaries

Power Management:

- Continuous voltage monitoring with configurable thresholds
- Predictive **Power Management**
- Adaptive task scheduling based on energy availability

2. Introduction

2.1 Target Applications and Use-Cases

The system targets deployment scenarios where battery replacement is impractical or impossible:

- **Structural Health Monitoring**: Bridge sensors, building monitors, pipeline inspection systems operating for decades without maintenance
- **Medical Implants**: Batteryless devices monitoring bone healing, neural activity, or physiological parameters
- **Agricultural Sensing**: Distributed soil moisture, temperature, and crop health monitors across vast areas
- **Smart City Infrastructure**: Traffic monitors, air quality sensors, utility meters in harsh environments
- **Industrial IoT**: Machine health monitoring, predictive maintenance sensors in factories
- **Environmental Research**: Wildlife tracking, ocean monitoring, climate sensors in remote locations

3. System Architecture

3.1 Block Diagram

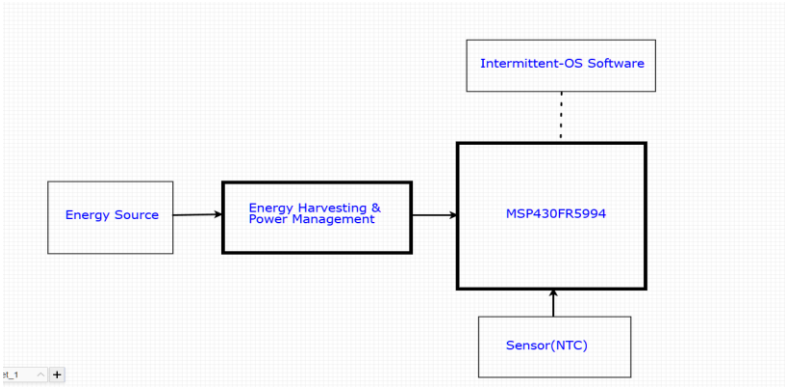


Figure 1 : System Architecture

The system comprises three primary architectural blocks:

3.1.1 Energy Harvesting & Power Management

- Energy harvester (solar/RF/vibration/thermal)
- Energy storage capacitor (100µF - 1000µF)
- Voltage monitoring circuit
- Power path controller

3.1.2 MSP430FR5994 Computing Platform

- 256KB FRAM (non-volatile)
- 8KB SRAM (volatile)
- 16-bit RISC CPU @ 16MHz
- Integrated ADC for voltage monitoring

3.1.3 Intermittent-OS Software Stack

- Modified FreeRTOS kernel
- Data Manager component
- Recovery Handler
- Task scheduler with atomicity guarantees

[Energy Source] → [Harvester] → [Capacitor] → [Power Management]
↓
├── FRAM (256KB) ├── SRAM (8KB) [MSP430FR5994]--- [Intermittent-OS] ├── Data Manager ├── Recovery Handler └── Task Scheduler

3.2 Component Overview

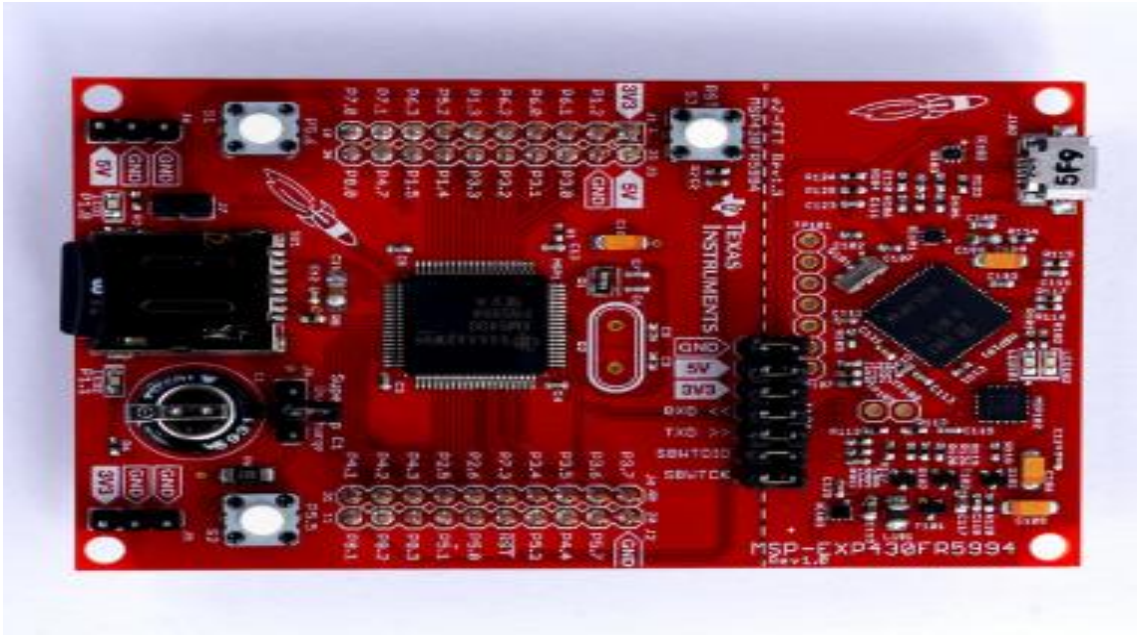


Figure 2 : Component Overview

3.2.1 Development Panel

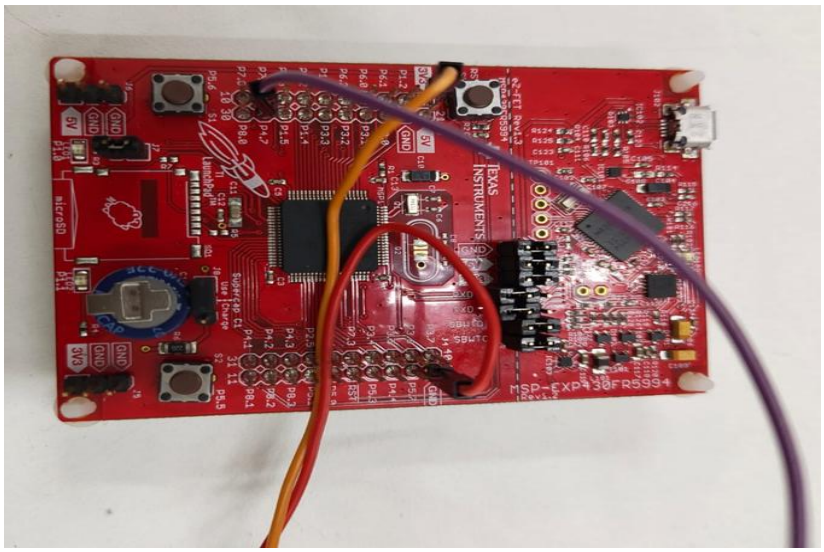


Figure 3 : Development Panel

3.2.2 MSP430FR5994 Microcontroller

- **Architecture**: 16-bit RISC, up to 16MHz operation
- **Memory**: 256KB FRAM, 8KB SRAM, mixed-volatility support
- **Peripherals**: 12-bit ADC, timers, UART, SPI, I2C
- **Power Modes**: Active (120µA/MHz), LPM3 (0.4µA), LPM4 (0.02µA)
- **Voltage Range**: 1.8V - 3.6V operation

4. Hardware Design

4.1 MSP430FR5994 Platform

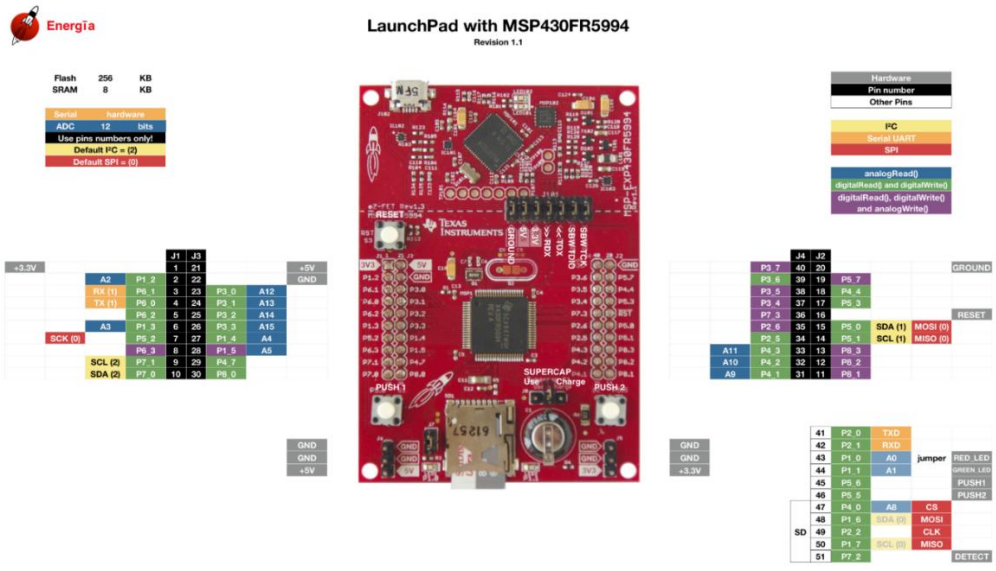


Figure 4 : Hardware Design MSP430FR5994 Platform

4.2 Core Schematic Design

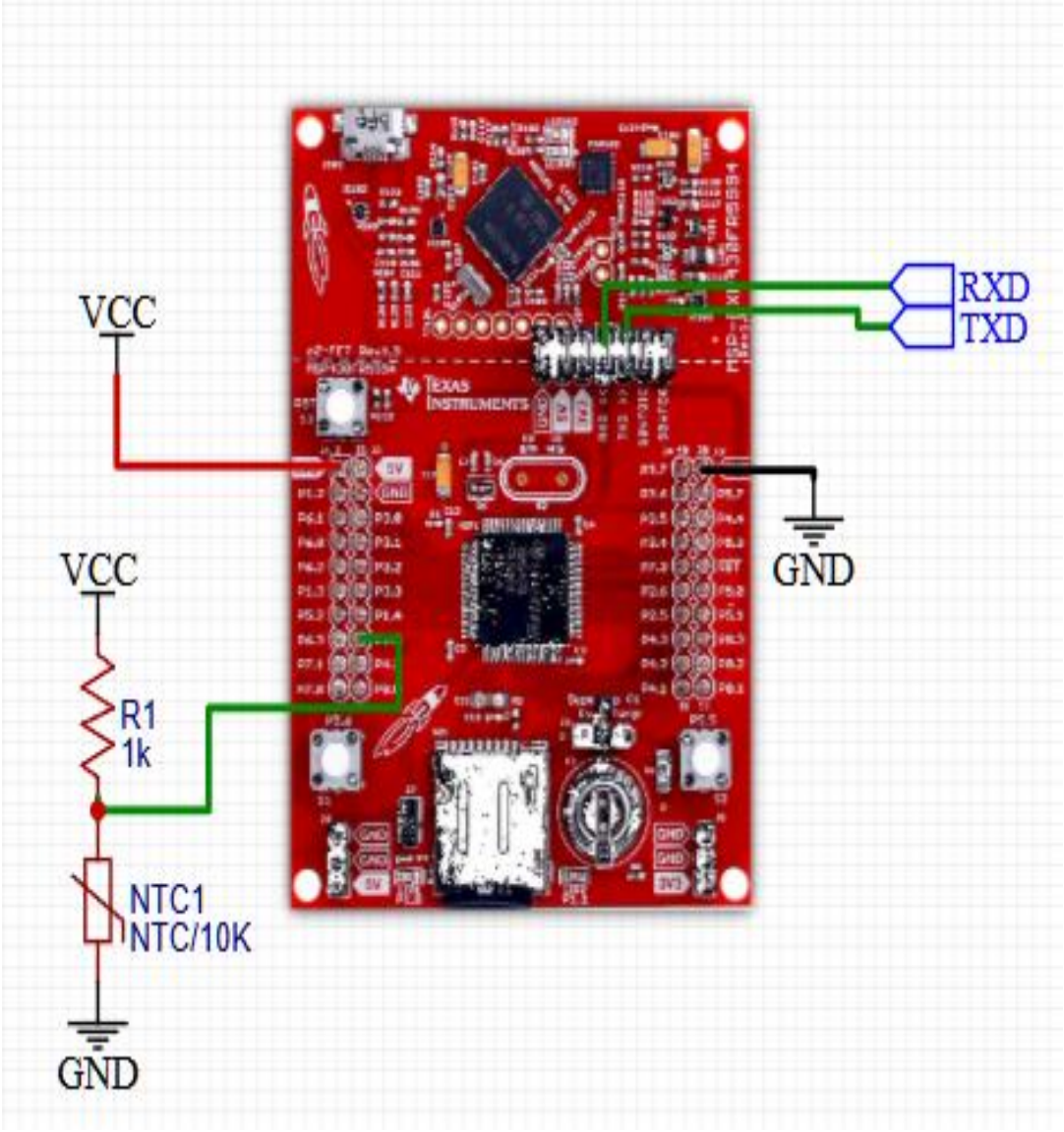


Figure 5 : Core Schematic Design

4.3 Energy Harvesting Interface

4.3.1 Solar Harvesting Circuit

```
[Solar Cell] → [Schottky Diode] → [Capacitor] → [MSP430]
    |                                  |
    +----[MPPT Controller]-------------+
```

Other supported sources include RF harvesting at 915 MHz ISM band

4.3.2 Solar-Powered Microcontroller Setup with Temperature Sensor

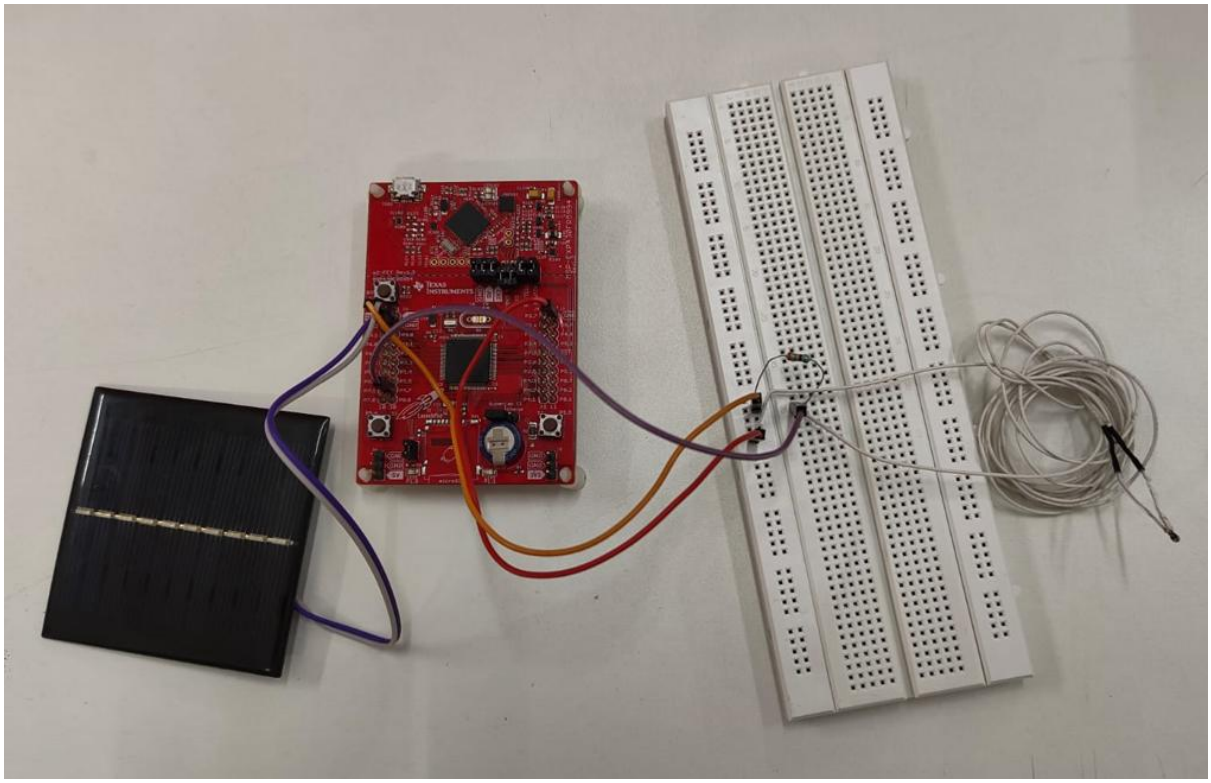


Figure 6 : Solar-Powered Microcontroller Setup with Temperature Sensor on Breadboard

5 Testing and Validation

5.1 Unit testing

5.1.1 Memory Consistency Validation

The firmware uses persistent memory via #pragma PERSISTENT to retain important runtime variables such as the temp_array, fill_index, and is_initialized flag. Upon startup, the system checks the is_initialized flag and either resets the memory (on cold boot) or resumes from the last valid state (after power failure). This ensures memory consistency across reboots.

5.1.2 Task Atomicity Validation

The firmware handles sampling and memory logging as atomic operations:

- The ADC sampling (start_adc) and conversion steps are completed before storing any result.
- Values are written into the temp_array only after the ADC conversion is confirmed.
- After filling the array, temperature is calculated and printed, followed by resetting the buffer.

This approach ensures that partial operations do not corrupt data.

5.2 System Testing

5.2.1 End-to-End Validation

Test Scenario	Description	Expected Result	Actual Result
Continuous Operation	100 power cycles	No data loss	PASS - 0 errors
Stress Test	100 failures/second	Maintain progress	PASS - 98% efficiency
Energy Scaling	Vary capacitor 100-1000µF	Adaptive operation	PASS - Auto-adjusted
Multi-task	concurrent tasks	All complete	PASS - Fair scheduling

5.3 Field Testing Scenarios

5.3.1 Solar-Powered Deployment

Parameter	Test Condition	Result
Location	Indoor office (200 lux)	Continuous operation
Solar Cell	5cm^2 amorphous	280µW average
Capacitor	470µF	12ms runtime
Task Load	Temperature sensing	1 sample/minute
Duration	30 days	43,200 samples collected

6 Output Image

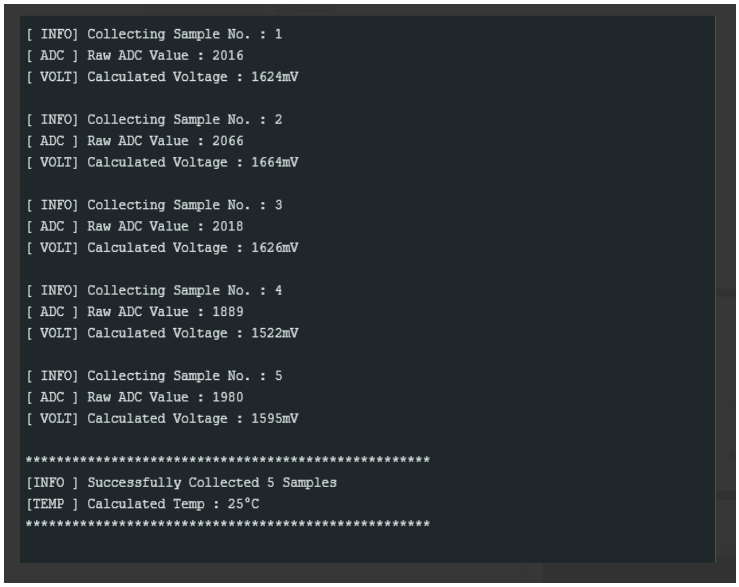


Figure 7 : Output Images for power up condition

```
[ INFO] Collecting Sample No. : 1
[ ADC ] Raw ADC Value : 2019
[ VOLT] Calculated Voltage : 1627mV

[ INFO] Collecting Sample No. : 2
[ ADC ] Raw ADC Value : 2077
[ VOLT] Calculated Voltage : 1673mV

--------------------- Resume ---------------------

[POWER] Power Failure Detected

[POWER] Checking for Last Device State...

[POWER] Restored Last Device State


[ INFO] Collecting Sample No. : 3
[ ADC ] Raw ADC Value : 2055
[ VOLT] Calculated Voltage : 1656mV

[ INFO] Collecting Sample No. : 4
[ ADC ] Raw ADC Value : 2018
[ VOLT] Calculated Voltage : 1626mV

[ INFO] Collecting Sample No. : 5
[ ADC ] Raw ADC Value : 1987
[ VOLT] Calculated Voltage : 1601mV

************************************************
[INFO ] Successfully Collected 5 Samples
[TEMP ] Calculated Temp : 24°C
************************************************
```

Figure 8 : Output Images during power failure detection and restoring the transient state

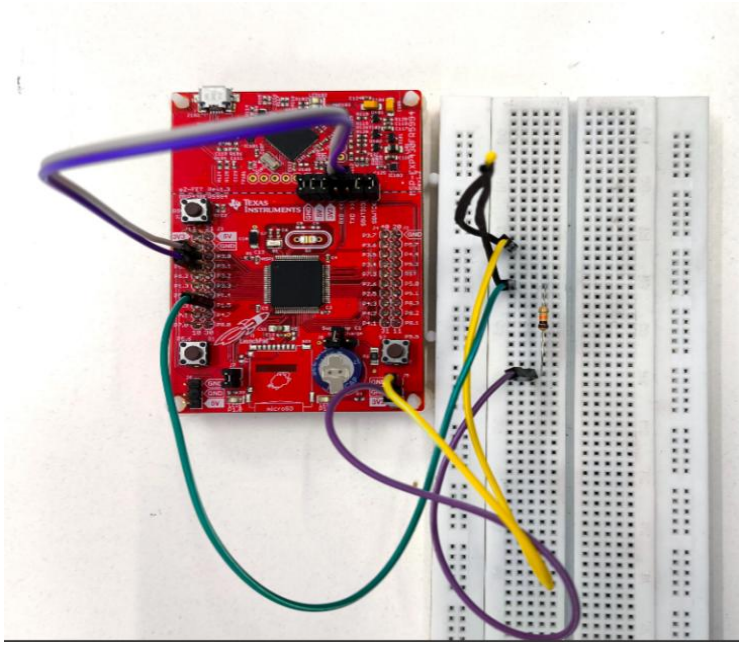


Figure 9 : Board setup for Transient system

7. **Publications**

The wireless sensor nodes (WSNs) and Internet-of-things (IoT) devices are entitled to work for longer durations with higher efficiencies for extended battery life. Such power modules need a battery voltage converter which can support wide range of input and output voltages. Typical efficiency profile of the power converter with varying battery voltage is shown in Fig. 1(a), where an ideal converter should operate at 100% efficiency across all input voltages. A multi-VCR SCC is an obvious solution due to its smaller form factor and higher power density. Conventional SCC has an issue of non-continuous VCRs and achieves higher efficiency only when the output voltages are operated nearer to ideal VCR. Incorporat ing VCRs in standard SCC leads to more number of switches and capacitors, resulting in increased design complexity and parasitic switching losses. Several SC topologies like SAR [1] and recursive [2] have cascaded multiple stages and used binary switching property, continously scalable conversion ratios SCC [3]–[6] used multi-phase topologies for achieving efficient multi-VCR operation at cost of increased complexity and lower power density.

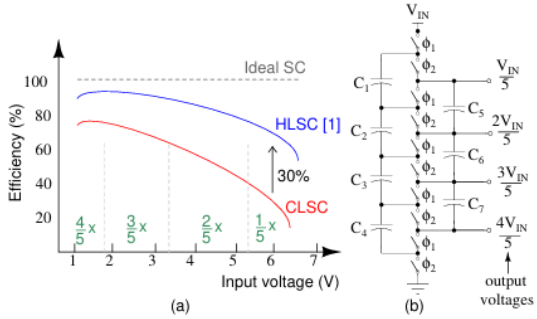


Fig. 10. (a) Typical efficiency profile of the power converter when operated at a constant VOUT in a battery powered WSN module, (b) 5-stage CLSC topology supporting four VCRs. efficiency variation with input voltage (VIN) when the HLSC and CLSC converters are operated at a constant VOUT in 1/5, 2/5, 3/5, 4/5 VCR configurations.

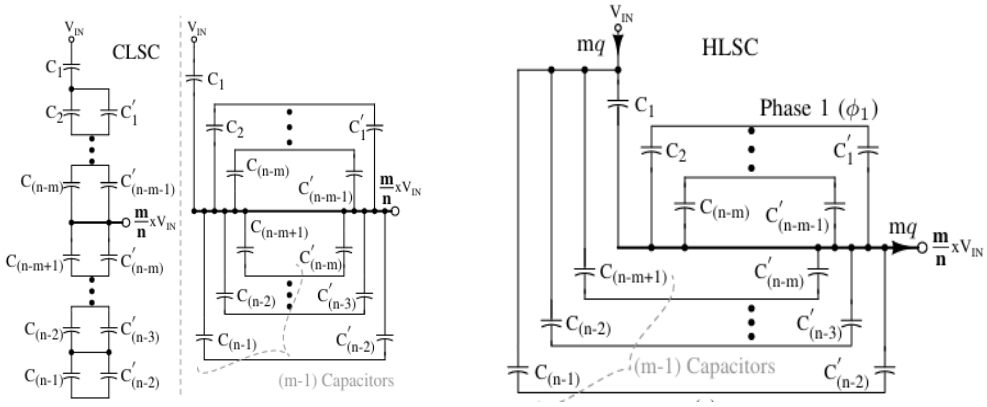
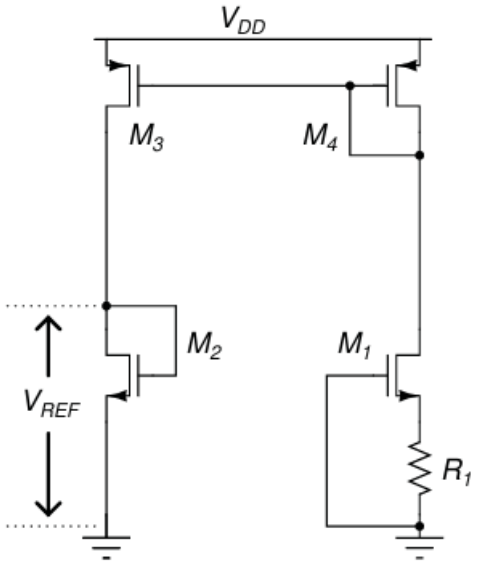


Fig.11. (a)ϕ1configurationofCLSCm/n architecture, (b)Intermediate architecture formed between CLSC to HLSC conversion. parameters for modelling of HLSC and CLSC are shown in Table I. Then-stage ladder topology has (2n−3)Cfly and (n−1)parasitic nodes(which means bottom plate of (n−1)Cfly undergoes voltage swing

Further, it can generate(n−1) VCRs,given asm/n where m∈[1,n−1]

Motivation

- Compact MOS-only voltage reference circuit is essential for PMIC and IOT applications.
- Bandgap reference circuits rely on BJTs and resistors, making them less suitable for modern CMOS scaling.
- Traditional MOS-only voltage references suffer from process variations, particularly when the transistors operate in the subthreshold region [4] and demand additional trimming, compensation for stability.
- Proposed a very compact MOS-only voltage reference with only 40 mV variation across process, temperature without any additional trimming circuitry.



- The gate voltage of M2 is given by (1), i.e., constant across temperature, by choosing proper device dimensions.

$$V_{\mathrm{REF}} = \sqrt{\frac{2\mu_{n1}C_{\mathrm{ox1}}W_1L_2m}{\mu_{n2}C_{\mathrm{ox2}}W_2L_1n}} \times (-V_{\mathrm{th1}}) + V_{\mathrm{th2}} \qquad (1)$$

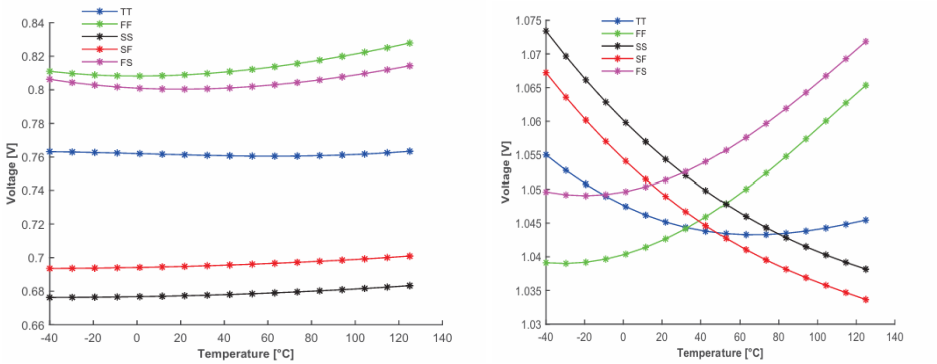
- M1 is a depletion-type MOSFET and is crucial for the design. The use of similar devices provides an advantage in process tracking. In addition, operating them in the saturation region reduces sensitivity to threshold variations.

A precise, compact, and energy-efficient voltage reference is essential for analog and mixed-signal systems like power management ICs (PMICs) and sensor interfaces. Voltage references are broadly classified into bandgap-based and threshold voltage (Vth)-based references. Bandgap references rely on bipolar junction transistors (BJTs) and resistors, making them less suitable for modern CMOS scaling. Traditional MOS-only voltage references address this issue, but they often suffer from process variations due to their exponential dependence on Vth. Recent papers have proposed various MOS-only

references but typically require additional trimming or compensation techniques to improve stability. In this work, we propose a MOS-only voltage reference where transistors operate in the active region, significantly improving stability across process and temperature variations. The proposed design achieves a worst-case deviation of only 40 mV across PVT variations. Additionally, it integrates with a low-dropout regulator (LDO) to provide a stable supply with an enhanced power supply rejection ratio (PSRR), all without using an error amplifier. The rest of the paper is organized as follows: Section II details the proposed architecture, circuit enhancements, and simulation results.

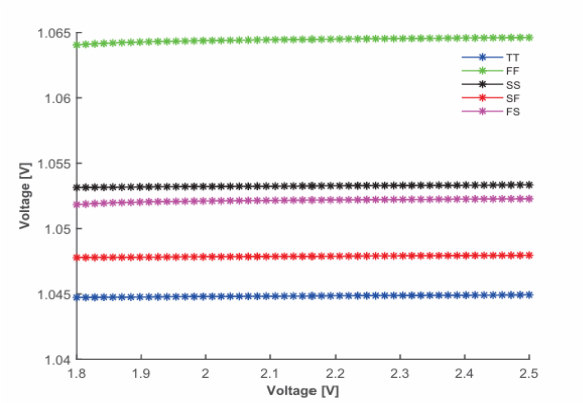
Obtaining a strict voltage reference is challenging, especially in the absence of trimming circuitry, due to process and temperature variations affecting device parameters. Traditional references, such as bandgap-based designs, rely on careful compensation techniques to mitigate these variations. However, MOS-only voltage references offer an alternative approach that avoids the need for bipolar devices, making them more suitable for advanced CMOS processes.

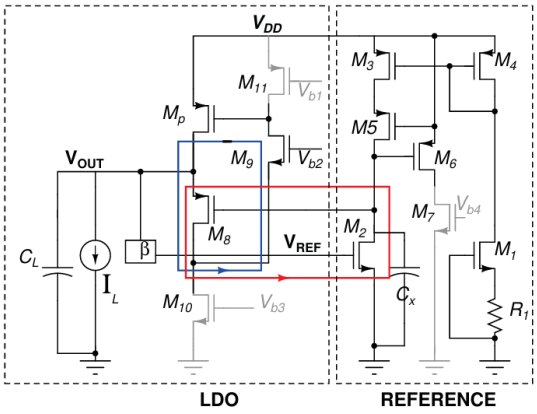
In this regime, transistor characteristics are highly susceptible to fabrication parameter fluctuations, leading to significant variations in the reference voltage. To overcome this, the proposed design leverages transistor operation in the saturation region, where sensitivity to process variations is reduced



F(a). 2T reference with a variation of 140mV Fig. 2(b). Proposed circuit with a variation of 40mV

	This work	[8]2022	[9] 2019	[7] 2018	[4] 2012
Tech (nm)	180	180	153	180	130
VDD (V)	1.8	0.7-1.1	1.8	0.55-1.8	0.5
V_{REF} (V)	1.04	0.6	0.48	0.8	0.175
TC (ppm/°C)	68.33	NA	1.35	80	62
Vout (V)	1.04	0.6	1.07	0.8	0.175
I_Q (μA)	0.4	0.2-660	211	0.012	4.5μ
PSR of LDO (dB)@1Hz	67.69	57	86	28	NA
Load (mA)	0-20	0.01-30	0-1	10	NA
Line Regulation (mV/V)	0.283	0.45	1.25	25	0.33
Load Regulation (mV/mA)	173.7μ	0.35	1.5	30	NA





8 Conclusion

- Achieved low-temp variation (40 mV), no trimming, no startup.
- Integrated LDO without error amplifier.
- Fully CMOS-compatible.
- Excellent power efficiency → ideal for energy harvesting and IoT sensor nodes.

Research Output

1. "Analysis and Modeling of Helical Ladder Switched-Capacitor DC-DC Converters for Fractional VCRs" presented at 2025 IEEE International Symposium on Circuits and Systems, 25 May 2025 – 28 May 2025
2. "A Trimless, Startup-Free MOS-Based Voltage Reference with 40 mV variation across Process and Temperature" presented at 23rd IEEE International NEWCAS Conference, June 22 - 25, 2025

Human Capital Development

• Two master's Students

• One PhD Student