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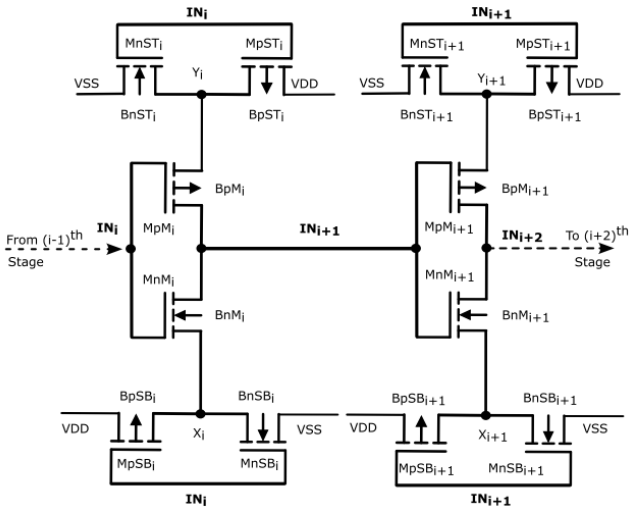
Activity Results Report:

"Design & Development of Energy Harvesting solution for Environment Sensor"

Ultra-low voltage start-up clock generators for micro-scale energy harvesting: New variants of body-biased stacked inverter based ring oscillators

In recent years, sensor network systems called Machine to Machine (M2M) and Internet of Things (IoT) have attracted a lot of attention. In such a sensor network system, communication is performed between a terminal that collects sensor data called an individual sensor node terminal and a server that collects the data. To realize an autonomous sensor network by using a power source that uses energy harvesting has attracted attention. As commercialization of energy-harvesting technology is progressing, the demand for ultra-low-voltage circuits has become higher.

This work aims to discuss the challenges of implementing an integrated ultra-low voltage start-up clock/oscillator, the state of the art and propose four new variants of a body-biased stacked inverter-based ring oscillator and analyze the same. The proposed delay cells designed in 180-nm BCD CMOS process are connected to form a 13-staged ring oscillator (RO) with regular Vt transistors. All four proposed variants' performance is compared against the former works (implemented in the same process) with respect to the lowest supply voltage required for sustained oscillations, oscillation frequency and peak-to-peak voltage swing (Vpp). For a supply voltage of 50 mV, over 90% VDD is obtained from post layout simulations for all four proposed architectures consuming around 24 pW of average power, out of which the variant that has the maximum swing of 92% (an improvement of 9.2% compared to that of stacked inverter-based RO), can start and sustain an oscillation at 32.5 mV supply voltage. The fastest architecture proposed has a frequency (post layout) of 131.5 Hz at 50 mV VDD, which is 62% more than that of the stacked inverter-based RO with body bias. Monte Carlo analysis reveals that the proposed RO variants' Vpp have lesser interquartile range (IQR) and relatively higher median values.



Peak-to-peak voltage swing and minimum supply voltage required for sustained oscillations for all types.

RO type	V_{pp} at V_{DD} = 50 mV	$V_{DD_{min}}$
NN-NN-NN	46 mV	32.5 mV
XX-NN-YY	45.45 mV	34 mV
SBBIRO	42.56 mV	37 mV
XX-XY-YY	45.23 mV	35 mV
SIRO	41.41 mV	38 mV
XX-GS-YY	45.02 mV	36 mV

Schematic versus post-layout frequency comparison.

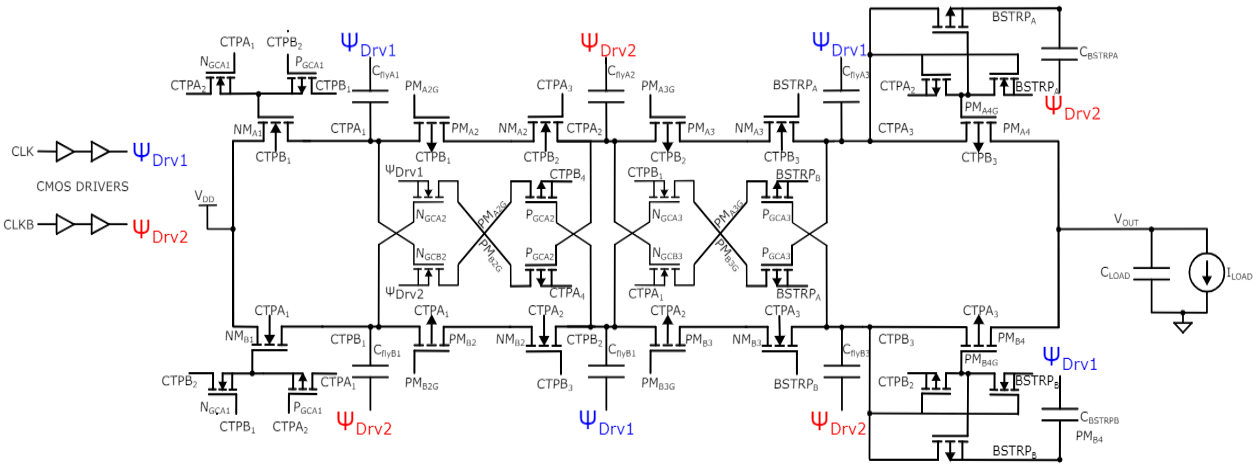
RO type	Schematic frequency	Post-layout frequency
NN-NN-NN	46.7 Hz	42.2 Hz
XX-NN-YY	97 Hz	70.2 Hz
SBBIRO	115.6 Hz	81.1 Hz
XX-XY-YY	136.1 Hz	108.2 Hz
SIRO	164.8 Hz	131.1 Hz
XX-GS-YY	167.5 Hz	131.5 Hz

High-Efficiency CMOS Charge Pump for Ultra-Low Power RF Energy Harvesting Application

One critical component of RF energy harvesting systems responsible for converting the DC voltage generated by the rectifier into a higher voltage suitable for powering the IoT device is the charge pump. The efficiency of the charge pump is critical to the overall performance of the energy harvesting system. A high-Power Conversion Efficiency (PCE) ensures that the maximum amount of energy is transferred from the RF signal to the energy-storage element, minimizing power losses and increasing the lifespan of the battery-free system. Optimizing the conduction and switching losses can improve the PCE of the charge pump

This paper explains the design and implementation of a switch capacitor DC-DC converter system for Radio Frequency (RF) energy harvesting applications for an input voltage in the sub-150mV range, using 180-nm CMOS triple- well BCD technology. The proposed system incorporates a charge pump architecture that employs an improvised Dynamic Gate Biasing (DGB), Forward and Reverse Body Bias technique (FRBB), along with a time axis symmetrical clocking scheme implemented using an advanced bootstrapped CMOS driver to enhance the overall drive capability of the system at low input voltages. Post-layout extracted simulations demonstrate that the proposed system achieves higher overall efficiency, delivering a peak Power Conversion Efficiency (PCE) of 85.8% at 125mV input voltage, outperforming other state-of-the-art architectures in similar voltage ranges. Moreover, the proposed system exhibits reliable operation even at input voltages as low as 85mV, while maintaining good overall efficiency.

The high efficiency obtained from the time-axis symmetric clocking scheme suggests the possible extension of the proposed architecture to AC inputs, representing a potential avenue for future research. We believe that the insights gained from this study can contribute to the development of more efficient and reliable power management systems for low-power applications.



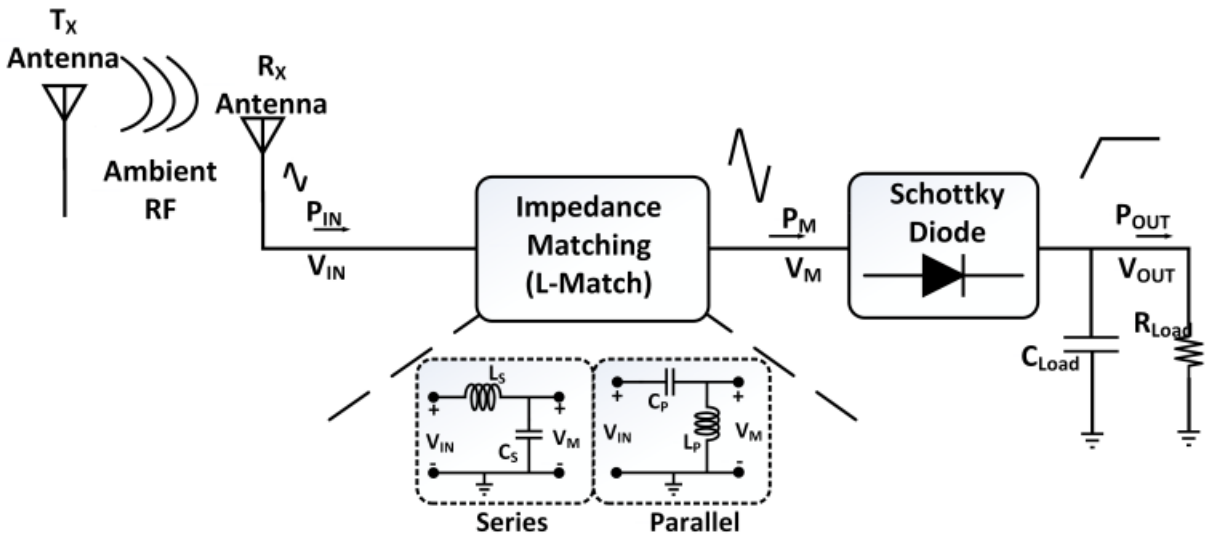
COMPARISON WITH PRIOR ART

Reference	*TCAS2'22* [5]	*Sensors'23* [9]	*TCAS1'14* [10]	*TCAS2'18* [11]	*TCAS2'20* [4]	This Work
Process	65nm	180nm	130nm	65nm	65nm	180nm
Implemented Scheme	ADGB	DGB & DBB	DBB	Bootstrap	DGB	DGB, FRBB & Bootstrap
No. of Stages	3	3	3	3	3	3
Frequency	4MHz	1MHz	250KHz	15.2MHz	25MHz	100KHz
Min. Input Voltage	100mV	100mV	180mV	150mV	200mV	85mV
Device Type	Low V_{TH}	Low V_{TH}	Low V_{TH}	Low V_{TH}	Low V_{TH}	Standard V_{TH}
Peak %PCE	43.4	33.8	34	38.8	78.2	85.8
Peak %VCE	86.5	95	85.97	80	99.4	84.1
Total Capacitors	82pF	60pF	60,000pF	22.5pF	100pF	125pF

Analysis of L-Matching Networks for Efficient Radio Frequency Energy Harvesting

An analytical design framework for a lumped (Inductor and Capacitor) L matching network for a Schottky diode series rectifier is presented in this study, which also demonstrates that a high pass network is more effective than a low pass network due to greater harmonic suppression. Passive component(L&C) values are derived in a close form equation and utilized to analyze component quality factor effects on rectifier performance. The theoretical predictions are verified by simulation for a multiple diode rectifier (SMS7630, HSMS2850, HSMS2862), which results in an improvement in HP network efficiency of 3 to 5 percent on average throughout a power range of -26 dBm to 12 dBm at a 915MHz frequency. This study confirms the suggested approach using measurement data developed on FR4 substrate and achieves 78% peak efficiency at 6dBm input power along with 38dB of dynamic range for > 20% efficiency from -26 dBm to +12dBm in an area of 1.8 X 2 cm2.

A wide input power range rectifier for harvesting ambient radio frequency energy from 915MHz ultra-high frequency has been proposed. This brief also demonstrates that a high pass network is more effective than a low pass network due to greater harmonic suppression. The presented prototype has only fabricated for SMS7630 to target low power range. The research can be further improved by fabricating multi diode approach to show wide input power range.



PERFORMANCE OF THE PROPOSED RECTENNA WITH REPORTED LITERATURE

Ref	Freq. (GHz)	Rectifier Topology	Diode Used	Peak Eff. (%) @ P_{IN} (dBm)	Power Range (>20%)	Dynamic Range (dB)	Rectifier Dim. (cm^2)
[10]	0.9, 1.8	Half Wave	SMS-7630	41 @ -10	-24 to -10	14	8.4 X 3.5
[11]	0.57 - 0.9	Half Wave	HSMS-2860	75 @ 15	-7 to 18	25	0.15 X 0.22 (\lambda)^2
[12]	0.85, 1.77, 2.07	Half Wave	HSMS-2850	61.9 @ 0	-21 to 5	26	0.29 X 0.08 (\lambda)^2
[8]	0.9, 1.8, 2.4	Half Wave	HSMS-2860	30 @ -8	-20 to 0	20	NA
[9]	0.9	Voltage Doubler	SMS-7630	65 @ 0	-15 to 7	22	NA
[5]	0.9, 1.8	Half Wave	HSMS-2850 HSMS-2862, SMS-7630	70 @ 2	-25 to -5	30	NA
This Work	**0.9**	**Half Wave**	**SMS-7630, HSMS-2850 HSMS-2862**	**78 @ 6**	**-26 to 12**	**38**	**1.8 X 2**
This Work (Parallel - Fabricated)	**0.9**	**Half Wave**	**SMS-7630**	**68 @ -6**	**-25 to 2**	**27**	**1.8 X 2**

Problem/constraints:

• Due to the pandemic effect on the semiconductor supply chain, we have had difficulty in procuring the components for the experiments effecting the timelines but nevertheless we have exhaustively worked towards the results for the research carried out.

Research Output:

• Mukherjee, Ankur, Ashik C. Jayamon, and Ashudeb Dutta. "Ultra-low voltage start-up clock generators for micro-scale energy harvesting: New variants of body-biased stacked inverter-based ring oscillators." Microelectronics Journal (2023): 105883. (https://doi.org/10.1016/j.mejo.2023.105883) 2.2 Impact Factor

• Mukherjee, Ankur, Ashik C. Jayamon, and Ashudeb Dutta. " High-Efficiency CMOS Charge Pump for Ultra-Low Power RF Energy Harvesting Application." Under Review Integration VLSI Journal 1.9 Impact Factor

• Deepali Pathak, Harshavardhan, and Ashudeb Dutta. " Analysis of L-Matching Networks for Efficient Radio Frequency Energy Harvesting." Under Review IEEE TCAS-II Express briefs Journal 4.4 Impact Factor

Human Capital Development:

• Two PhD Students
• Two Design Engineers
• Two Layout Engineers